(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 237 099 A1

(12) EUROPEAN PATENT APPLICATION
published in accordance with Art. 158(3) EPC

(43) Date of publication:
04.09.2002 Bulletin 2002/36

(21) Application number: **00974849.2**

(22) Date of filing: **08.11.2000**

(51) Int Cl.[7]: **G06F 17/50**

(86) International application number:
PCT/JP00/07869

(87) International publication number:
WO 01/037148 (25.05.2001 Gazette 2001/21)

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR

(30) Priority: **18.11.1999 JP 32779699**

(71) Applicant: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
Kadoma-shi, Osaka 571-8501 (JP)

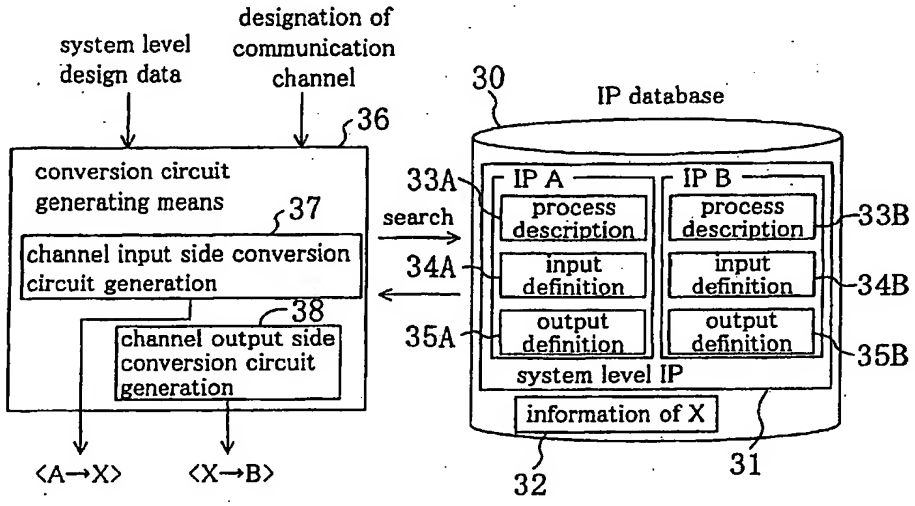
(72) Inventors:
- **OKAZAKI, Kaoru**
  Higashiosaka-shi, Osaka 578-0901 (JP)
- **MIZUNO, Masanobu**
  Takatsuki-shi, Osaka 569-1042 (JP)
- **MURAOKA, Michiaki**
  Nakano-ku, Tokyo 164-0013 (JP)

(74) Representative: **Weigelt, Udo**
Grünecker, Kinkeldey
Stockmair & Schwanhäusser
Anwaltssozietät
Maximilianstrasse 58
80538 München (DE)

(54) IP BASE LSI DESIGNING SYSTEM AND DESIGNING METHOD

(57) An IP database (**30**) includes a system level IP (**31**) used in system level design. IPs **A** and **B** in the system level IP (**31**) are divided into processing algorithm description portions (**33A** and **33B**), input data structure definition portions (**34A** and **34B**) and output data structure definition portions (**35A** and **35B**). When a communication channel is provided between the IPs communicating data in architecture or functional design, a conversion circuit generating means (**36**) generates a data conversion circuit between the communication channel and each of the IPs with reference to the IP database (**30**).

Fig. 3



EP 1 237 099 A1

Description

Technical Field

[0001] The present invention belongs to a technology relating to a so-called IP-based LSI design.

Background Art

[0002] Conventionally, integrated circuit devices within electronic appliances have been manufactured by forming individual LSIs of different types, for example, memory and processor, on semiconductor chips and then mounting the chips on a base substrate such as a printed circuit board.

[0003] Recently, however, there is a higher demand for miniaturized, lightweight, power-saving and low-cost integrated circuit devices used in electronic appliances, for the purpose of wider-ranging utilization of the electronic appliances. This trend is even more pronounced in the field of digital information household appliances. And in response to this trend, semiconductor manufacturers are forced to shift their emphasis on research and development from memories toward system LSIs.

[0004] Specifically, such system LSIs are realized by a so-called system-on-chip solution with the memory and a variety of logic circuits provided on a single chip. For the system-on-chip solution, process technology is required for forming elements having different structures on a common substrate, but also the design technology therefor needs to be revolutionized.

[0005] Thus, a so-called IP-based method of preparing data (IPs) for designing so-called functional blocks realizing certain functions and using these data to design a desired system LSI as a combination of the respective functional blocks has been proposed as the design technology suitable for this system-on-chip solution. When such a design method is used, the respective functional blocks already have predetermined configurations for realizing their functions, so that the integrated circuit device can be designed just by designing the wiring among the respective functional blocks, and designing the peripheral circuits. With such a design method, design efficiency can be improved significantly.

[0006] However, the above-described IP-based LSI design method has the following problems.

[0007] When shifting from system level design to architecture design or functional design, a communication channel between the IPs is also given a concrete form. Thus, consideration must be given to data consistency between each of the IPs and the communication channel, which increases design man-hours. Moreover, when an IP that realizes a certain function is selected, it is very rare that the selected IP can be used for an LSI to be newly designed as it is, and considerable design man-hours are necessary for new designs, revisions and verifications. Furthermore, a power control circuit exclusively used for the LSI needs to be designed manually, so that design efficiency is low.

Disclosure of Invention

[0008] It is an object of the present invention to reduce design man-hours and improve design efficiency in IP-based LSI design.

[0009] Specifically, as an IP-based LSI design system, the present invention includes an IP database having a system level IP used in system level design, and in the system level IP, each IP is described divided into a processing algorithm description portion describing a processing algorithm of the IP, an input data structure definition portion representing a structure definition of input data serving as a processing unit, and an output data structure definition portion representing a structure definition of output data serving as a processing unit.

[0010] It is preferable that the IP-based LSI design system further includes a means for generating a conversion circuit that converts data for communication between a communication channel and the system level IPs, when the communication channel is provided between the system level IPs performing data communication in architecture design or function design.

[0011] Furthermore, when the communication channel is provided between first and second system level IPs communicating with each other, the conversion circuit generating means preferably searches the IP database, reads out descriptions of the output data structure definition portion in the first system level IP and the input data structure definition portion in the second system level IP, and generates the conversion circuit based on the read out descriptions. Then, it is preferable that the IP database further includes an IP for the communication channel and that, when the communication channel is provided between the first and the second system level IPs, the conversion circuit generating means searches the IP database and further reads out input/output data structure definitions of the IP for the communication channel. Alternatively, when input/output data structures are different between the first and the second system level IPs, the conversion circuit generating means preferably generates the conversion circuit in accordance with information representing a correspondence between the input/output data structures.

[0012] Moreover, it is preferable that the conversion circuit converts the amount of data per communication unit. Alternatively, it is preferable that the conversion circuit preferably a conversion between address data indicating a data area and actual data corresponding to the address data.

[0013] Furthermore, as an IP-based LSI design method the present invention uses an IP database having a system level IP used in system level design, and in the system level IP, each IP is described divided into a processing algorithm description portion describing a processing algorithm of the IP, an input data structure definition portion representing a structure definition of

input data serving as a processing unit, and an output data structure definition portion representing a structure definition of output data serving as a processing unit.

[0014] It is preferable that the IP-based LSI design method includes a step of generating a conversion circuit that converts data for communication between a communication channel and the system level IPs, when the communication channel is provided between the system level IPs performing data communication in architecture design or function design.

[0015] Furthermore, when the communication channel is provided between a first and a second system level IPs, it is preferable that in the conversion circuit generation step, the IP database is searched, descriptions of the output data structure definition portion in the first system level IP and the input data structure definition portion in the second system level IP are read out and the conversion circuit is generated based on the read out descriptions.

[0016] It is preferable that the IP database further includes an IP for the communication channel and that when the communication channel is provided between the first and the second system level IPs, in the conversion circuit generation step, the IP database is searched, and input/output data structure definitions of the IP for the communication channel are further read out. Alternatively, when input/output data structures are different between the first and the second system level IPs, it is preferable that in the conversion circuit generation step, the conversion circuit is generated in accordance with information representing a correspondence between the input/output data structures.

[0017] Moreover, it is preferable that the conversion circuit converts the amount of data per communication unit. Alternatively, it is preferable that the conversion circuit performs a conversion between address data indicating a data area and actual data corresponding to this address data.

[0018] Moreover, as an IP-based LSI design system, the present invention includes a function classification database in which an equipment configuration is classified into respective elements with regard to function and arranged systematically, and IP-based LSI design is carried out using the function classification database.

[0019] It is preferable that the IP-based LSI design system includes an existing design asset database in which IPs already generated are stored in association with respective elements in the function classification database, and that an IP suitable for an LSI to be designed is selected from the IPs stored in the existing design asset database with reference to the function classification database.

[0020] Furthermore, it is preferable that the IP-based LSI design system includes a design assets compatibility evaluation rule database that stores information for defining mutual compatibility between the IPs stored in the existing design asset database, and that compatibility of the IP selected for the LSI to be designed is evaluated with reference to the design assets compatibility evaluation rule database. Alternatively, it is preferable that the IP-based LSI design system selects an IP having a similar function to that of an IP suitable for the LSI to be designed from the IPs stored in the existing design asset database and revises the function of the selected IP so as that it becomes suitable for the LSI to be designed. Alternatively, it is preferable that the existing design asset database in the IP-based LSI design system includes a means for managing history information, such as a progenitor IP and differences from the progenitor IP, for each of the IPs to be stored.

[0021] Moreover, as an IP-based LSI design method, the present invention uses a function classification database in which an equipment configuration is classified into elements with regard to function and arranged systematically to perform IP-based LSI design.

[0022] It is preferable that the IP-based LSI design method uses an existing design asset database in which IPs already generated are stored in association with respective elements in the function classification database and that an IP suitable for an LSI to be designed is selected from the IPs stored in the existing design asset database with reference to the function classification database.

[0023] Furthermore, it is preferable that the IP-based LSI design method uses a design assets compatibility evaluation rule database that stores information for defining mutual compatibility between the IPs stored in the existing design asset database and that compatibility of the IP selected for the LSI to be designed is evaluated with reference to the design assets compatibility evaluation rule database. Alternatively, it is preferable that the IP-based LSI design method selects an IP having a similar function to that of an IP suitable for the LSI to be designed from the IPs stored in the existing design asset database and revises the function of the selected IP so that it becomes suitable for the LSI to be designed.

[0024] Moreover, as an IP-based LSI design system, the present invention includes a means for generating architecture level design data from a system level function definition regarding an LSI to be designed, a means for performing operation analysis of the LSI to be designed by using the generated architecture level design data and an operation pattern definition of the LSI to be designed, and a means for generating a power control block in the architecture level design data based on operation analysis results.

[0025] Furthermore, as an IP-based LSI design method, the present invention includes a step of generating architecture level design data from a system level function definition, a step of performing an operation analysis of the LSI to be designed by using the generated architecture level design data and an operation pattern definition of the LSI to be designed, and a step of generating a power control block in the architecture level design data based on operation analysis results.

Brief Description of Drawings

[0026]

Fig. 1 is a conceptual diagram illustrating IP-based LSI design.
Figs. 2(a) and 2(b) are diagrams schematically showing a conversion from a system level to an architecture level or to a functional level.
Fig. 3 is a diagram showing an example of a configuration for a main part of an IP-based LSI design system according to the first embodiment of the present invention.
Figs. 4(a) and 4(b) are diagrams showing an example of a generated data conversion circuit.
Figs. 5(a), 5(b) and 5(c) are diagrams showing another example of the data conversion circuit.
Fig. 6 is a diagram showing another example of the data conversion circuit.
Figs. 7(a) and 7(b) are diagrams schematically showing the conversion from the system level to the architecture level or to the functional level, in which conversion into a different data structure is made between IPs.
Fig. 8 is a diagram showing an example of a configuration for the main part of the IP-based LSI design system according to the first embodiment of the present invention.
Fig. 9 is a diagram showing an example of the generated data conversion circuit.
Fig. 10 is a diagram showing a configuration of an IP-based LSI design system according to the second embodiment of the present invention.
Fig. 11 is a diagram showing an example of the contents of a function classification DB.
Fig. 12 is a diagram showing an example of input data obtained by referring to the function classification DB.
Fig. 13 is a diagram showing an example of the contents of an existing design assets DB.
Fig. 14 is an example of IP information included in an existing design DB.
Fig. 15 is a diagram showing an example of the contents of a design assets compatibility evaluation rule DB.
Fig. 16 is a diagram showing a configuration of an IP-based LSI design system according to the third embodiment of the present invention.
Fig. 17 is a diagram showing an example of operation analysis results.

Best Mode for Carrying Out the Invention

[0027] Hereinafter, embodiments of the present invention will be described with reference to the drawings.

First Embodiment

[0028] Fig. 1 is a conceptual diagram illustrating IP-based LSI design. As shown in Fig. 1, IP-based LSI design is carried out hierarchically in the order of system level design **S11**, architecture design **S12**, functional design **S13**, logic design **S14** and layout design **S15**. In the system level design **S11**, the architecture design **S12** and the functional design **S13**, which are the upstream processes, an IP database **1** is utilized, which stores so-called IPs used for the LSI design.

[0029] The IP database **1** stores system level IPs **11** having information of the system level, behavior IPs **12** having information of the architecture level and RTL IPs **13a** or software IPs **13b** having information of the functional level, each of which is associated with a corresponding IP. In the system level design **S11**, the system level IP **11** is reused. In the architecture design **S12**, the behavior IP **12** corresponding to the reused system level IP **11** is retrieved via an interface **15**, whereas in the functional design **S13**, the RTP IP **13a** or the software IP **13b** corresponding to the reused system level IP **11** is retrieved via the interface **15**.

[0030] Figs. **2(a)** and **2(b)** are diagrams schematically showing a conversion from the system level to the architecture level or to the functional level. In the system level design, a system level IP **A** and IP **B** is reused, as shown in Fig. **2(a)**. In the architecture design or the functional design, lower-level IPs (an RTL IP **A** and IP **B** in this figure) corresponding to the system level IP **A** and IP **B** are retrieved from the IP database and reused as shown in Fig. **2(b)**.

[0031] However, since a communication channel (for example a bus) **X** is given a concrete form in the architecture design or the functional design, data conversion circuits **21A** and **21B** for properly connecting the input/output of the RTL IP **A** and IP **B** to the communication channel **X** have to be newly developed. In order to develop the data conversion circuits **21A** and **21B**, it is necessary to analyze the input/output of the system level IP **A** and IP **B** and verify the consistency of the input/output data. In other words, it is necessary not only to simply realize a processing algorithm but also to take "the consistency of the input/output data" into account.

[0032] As described above, although the RTL IP and the software IP can be retrieved easily by referring to the IP database, generation of the data conversion circuit requires design man-hours, and therefore, there is the problem that design efficiency cannot be improved. The invention according to this embodiment solves this problem and realizes a highly efficient IP-based LSI design.

[0033] Fig. 3 is a diagram showing an example of a configuration for a main part of the IP-based LSI design system according to this embodiment. A system level IP 31 in an IP database **30** shown in Fig. **3**, the IP **A** and the IP **B** are described divided into a processing algorithm description portions **33A** and **33B** describing the

processing algorithms of the respective IPs, input data structure definition portions **34A** and **34B** representing structure definitions of input data serving as processing units and output data structure definition portions **35A** and **35B** representing structure definitions of output data serving as processing units. An IP **32** representing information of the communication channel **X** is also stored in the IP database **30**. The IP **32** includes descriptions of definitions of input/output data structures of the communication channel **X**.

[0034] Taking an IP that performs YC separation as an example, the processing algorithm description portion, the input data structure definition portion and the output data structure definition portion store the following information, respectively. First, in the processing algorithm description portion, an algorithm of a process for separating an NTSC signal line by line into a luminance signal and a chrominance signal is described. Then, in the input data structure definition portion, a definition of a line of the NTSC signal to be inputted is described as, for example, "in [8] [525]." In the output data structure definition portion, definitions of the luminance signal and the chrominance signal to be outputted are described as, for example, "out 1 [4] [525], out 2 [4] [525]."

[0035] In accordance with the design data of the system level or the designation of a communication channel, a conversion circuit generating means **36** generates a data conversion circuit. At this time, the input data structure definition portions **34A** and **34B** and the output data structure definition portions **35A** and **35B** of the system level IP **31** in the IP database **30** as well as the communication channel IP **32** are searched.

[0036] Figs. **4(a)** and **4(b)** are diagrams showing an example of the data conversion circuit generated by the conversion circuit generating means **36**. Of these figures, Fig. **4(a)** shows an example of the data conversion circuit **21A** in the Fig. **2(a)**, and Fig. **4(b)** shows an example of the data conversion circuit **21B**. Herein, both of the RTL IP **A** and the IP **B** are IPs relating to image processing and are taken to input/output data line by line, whereas the communication channel **X** is taken to transfer data pixel by pixel.

[0037] When a channel input side conversion circuit generating portion **37** generates the data conversion circuit **21A** between the RTL IP **A** and the communication channel **X**, for example, it searches the output data structure definition portion **35A** in the system level IP **A** and information on the input data structure of the IP **32** for the communication channel **X**. Then, in accordance with the retrieved information, the size of a line buffer **41** is determined, an output selector **42** is generated and a control circuit **43** is generated as shown in Fig. **4(a)**. In the same manner, when a channel output side conversion circuit generating portion **38** generates the data conversion circuit **21B** between the communication channel **X** and the RTL IP **B**, it searches information on the output data structure of the IP **32** for the communication channel **X** and the input data structure definition portion **34B** in the system level IP **B**. Then, in accordance with the retrieved information, a distribution circuit **46** is generated, the size of a buffer **47** is determined and a control circuit **48** is generated as shown in Fig. **4 (b)**.

[0038] Figs. **5(a)** to **5(c)** are diagrams showing another example of the data conversion circuit. In Figs. **5(a)** to **5(c)**, it is assumed that the data word length per communication unit is converted. In Fig. **5(a)**, both of the RTL IP **A** and the IP **B** are taken to input/output data in 32-bit units and the communication channel **X** is taken to transfer data in 16-bit units. In this case, the data conversion circuit **21A**, which is provided with a 32-bit register **51**, a selector **52** and a control circuit **53** as shown in Fig. **5 (b)**, is generated between the RTL IP **A** and the communication channel **X**, whereas the data conversion circuit **21B**, which is provided with a 16-bit data distribution circuit **56**, a 32-bit register **57** and a control circuit **58** as shown in Fig. **5(c)**, is generated between the communication channel **X** and the RTL IP **B**.

[0039] Fig. **6** is a diagram showing another example of the data conversion circuit. In Fig, **6**, the RTL IP **A** has an internal memory **61** with a data length of 32 bit and is taken to output address data designating a location at which output data are stored in this internal memory **61**, and the communication channel **X** is taken to be able to transfer 32-bit data. In other words, Fig. **6** assumes conversion between the address data for designating the location at which the data are stored and the actual data. In this case, a data conversion circuit **21A** made of a DMA (Direct Memory Access) circuit is generated between the RTL IP **A** and the communication channel **X**, whereas a data conversion circuit **21B**, which is provided with a working memory **62** and an R/W control circuit **63**, is generated between the communication channel **X** and the RTL IP **B**.

[0040] For example, if the RTL IP **A** outputs "8000" as the address data, then the data conversion circuit **21A**, which is a DMA circuit, reads out data from the internal memory **61** successively in order from the address 8000. On the other hand, in the data conversion circuit **21B**, the R/W control circuit **63** writes a series of data to be transmitted successively from the communication channel **X** into the working memory **62** and outputs the address data indicating the location into which the data are written to the RTL IP **B**. Then, the RTL IP **B** accesses the working memory **62** to obtain the data.

[0041] Figs. **7(a)** and **7(b)** are diagrams schematically showing the conversion from the system level to the architecture level or to the functional level, in which conversion into different data structures is carried out between the IPs. In Fig. **7(a)**, output data of the system level IP **A** are taken to be in line units (50 pixels by 100 lines), whereas input data of the system level IP **B** are taken to be in sub-block units (40 pixels by 90 lines).

[0042] Fig. **8** is a diagram showing an example of a configuration for the main part of the IP-based LSI de-

sign system according to this embodiment, and corresponds to Figs. **7(a)** and **7(b)**. In addition to the design data of the system level and the designation of the communication channel, a conversion circuit generating means **36A** shown in Fig. **8** generates a data conversion circuit in accordance with information that indicates the correspondence between the data structures of the IP **A** output and the IP **B** input.

[0043] Fig. **9** is a diagram showing an example of the data conversion circuit generated by the conversion circuit generating means **36A**. A channel output side conversion circuit generating portion **38** searches the information on the output data structure of the IP **32** for the communication channel **X** and the input data structure definition portion **34B** in the system level IP **B**, and then generates a distribution circuit **71**, determines the size of a buffer **72**, generates a selector **73** and generates a control circuit **74** in accordance with the retrieved information, as shown in Fig. **9**.

Second Embodiment

[0044] When an applicable IP is selected by searching the IP database in IP-based LSI design, it is very rare that the selected IP can be used as is for the LSI to be newly designed. Actually, it seems that, in most cases, the selected IP is inappropriate because of specification problems, or even when it is applicable, revisions and verifications are required. This problem increases the design man-hours and hinders realization of the efficient LSI design.

[0045] With a so-called target-driven reuse and design method of allocating components in accordance with requirement specifications, this problems is inevitable. Therefore, the inventors of the present invention propose a so-called IP-DB-driven reuse and design method. This method classifies input data into structural elements for which the possibility is high that there are existing design assets (IPs), so that the existing IPs can be used efficiently.

[0046] Fig. **10** is a diagram showing a configuration of an IP-based LSI design system according to the second embodiment of the present invention. In this system, the steps **S21** to **S25** are realized by a program that is executed by a computer, for example.

[0047] First, in the input data generation step **S21**, input data are generated hierarchically with reference to a function classification DB **81**. Then, in the performance requirement assignment step **S22**, performance specifications are assigned to the various hierarchical elements of the input data.

[0048] Fig. **11** is a diagram showing an example of the contents of the function classification DB **81**. In the function classification DB **81**, equipment configurations are classified into a variety of elements with regard to their function and then arranged systematically, as shown in Fig. **11**. In the example shown in Fig. **11**, function classification is carried out for two types of digital video equipment. For example, the digital video equipment A is classified into an input interface part, a servo control part, a signal processing part, a system control part and an output interface part. The input interface part is further classified into a signal readout part, the signal processing part is further classified into an error correction part and an AV processing part, and the output interface part is further classified into an output signal generation part and a signal transmission part. The AV processing part is further classified into an AV separation part, a video processing part and an audio processing part.

[0049] Fig. **12** is a diagram showing an example of input data obtained through the input data generation step **S21** and the performance requirement assignment step **S22**. In the example shown in Fig. **12**, a digital TV/VCR combination is assumed as the object to be newly designed and is provided with digital television functions to which digital video functions are added as its specification **80**. As shown in Fig. **12**, in the input data generation step **S21**, a new function hierarchy is constructed as input data, based on the function classification in the function classification DB **81** as shown in Fig. **11**.

[0050] In the compatible design asset selection step **S23**, an IP suitable for an LSI to be designed is selected from IPs stored in an existing design asset DB **82** with reference to the function classification DB 81.

[0051] Fig. **13** is a diagram showing an example of the contents of the existing design asset DB **82**. As shown in Fig. **13**, in the existing design asset DB **82**, IPs that have already been generated are stored in correlation with respective elements in the function classification DB **81**. In Fig. **13**, blocks surrounded by squares show respective IPs whereas blocks circled by ellipses correspond to elements in the function classification DB **81**. For example, three types of IPs, "Reed-Solomon," "Viterbi" and "Trellis," are generated with respect to a function of "error correction."

[0052] In this case, input data are described hierarchically as shown in Fig. **12**, so that an IP may be selected from any hierarchy. In other words, there may be multiple choices regarding selection of the IP.

[0053] Then, in the compatibility evaluation step **S24**, compatibility of the selected IPs is evaluated with reference to the existing design asset DB **82** and the inter design assets compatibility evaluation rule DB **83**. That is to say, an optimal solution for the selection of the IP is obtained in view of cost, power consumption, operating speed and the like.

[0054] Fig. **14** is a diagram showing an example of IP information included in the existing design asset DB **82**. In Fig. **14**, data form, data display format, design method, design results and distributable objects for each of the IPs are described as the IP information.

[0055] Fig. **15** is a diagram showing an example of contents of the inter design assets compatibility evaluation rule DB **83**. As shown in Fig. **15**, the inter design assets compatibility evaluation rule DB 83 stores infor-

mation for defining mutual compatibility between the IPs stored in the existing design asset DB **82** as shown in Fig. **14**. Rules for defining compatibility include theoretical rules and empirical rules. Examples of the theoretical rules include "good consistency" and "prolongs the lifetime" for good compatibility, and "additional functions are required" and "specifications are not compatible" for poor compatibility. On the other hand, examples of the empirical rules include "many parts can be shared" and "consumption power can be reduced" for good compatibility, and "operation can not be verified" and "increases the area" for poor compatibility.

[0056] In the relevant design asset retrieval step **S25**, an IP having a similar function to that of a functional element for which no adequate IP was found is selected from the IPs stored in the existing design asset DB **82**. Then, the function of the selected IP is revised so that it becomes suitable for the functional element. Thereby, man-hours required for the functional revision can be considerably reduced.

[0057] The revised IP is registered in the existing design asset DB **82** as a newly generated IP. Moreover, the existing design asset DB **82** may be provided with a means for managing history information such as a progenitor IP and differences from the progenitor IP regarding each of the IPs to be stored.

Third Embodiment

[0058] Fig. **16** is a diagram illustrating the configuration of an IP-based LSI design system according to the third embodiment of the present invention. In this embodiment, a low-power system LSI (with reduced power consumption) can be realized by utilizing IPs efficiently in the top-down design of the system LSI.

[0059] First, in the system level design, a function definition **91** according to a system level IP is obtained with respect to the LSI to be designed. Next, in an architecture generation step **S31**, design data **92** of the architecture level are generated from the function definition **91** according to the system level IP. Then, in an operation analysis step **S32**, operation analysis of the LSI to be designed is carried out using these design data **92** of the architecture level, a command **93** and an operation pattern definition **94** that defines the operation of the system LSI.

[0060] Fig. **17** is a diagram showing an example of the operation analysis results. In Fig. **17**, it is necessary to supply power during operation, but it is unnecessary to supply power outside of operation so that in this case it is possible to turn the power off. Alternatively, a method of interrupting clock supply instead of turning the power off is also conceivable.

[0061] Then, in a power control function generation step **S33**, a power control block **CTL1** for the entire LSI and power control blocks **CTL2** to **CTL6** for respective IPs are generated in the design data of the architecture level based on the operation analysis results **95** (method 1). Alternatively, power control may be performed by adding a low-power command to the original command instead of generating the power control block **CTL1** for the entire LSI.

[0062] According to the present invention as described above, a data conversion circuit for communications can be generated easily, because each of the IPs in a system level IP is described divided into a processing algorithm description portion, an input data structure definition portion and an output data structure definition portion. Moreover, reuse efficiency of the IPs can be increased, because a function classification database, in which an equipment configuration is classified into respective elements with regard to function and arranged systematically, is used. Furthermore, power control blocks can be generated easily. Consequently, the design efficiency of IP-based LSI design can be further improved.

Claims

1. An IP-based LSI design system comprising an IP database having a system level IP used in system level design,
   wherein, in the system level IP, each IP is described divided into:
   a processing algorithm description portion describing a processing algorithm of the IP;
   an input data structure definition portion representing a structure definition of input data serving as a processing unit; and
   an output data structure definition portion representing a structure definition of output data serving as a processing unit.

2. The IP-based LSI design system according to claim 1,
   further comprising a means for generating a conversion circuit that converts data for communication between a communication channel and the system level IPs, when the communication channel is provided between the system level IPs performing data communication in architecture design or function design.

3. The IP-based LSI design system according to claim 2,
   wherein, when the communication channel is provided between first and second system level IPs communicating with each other, the conversion circuit generating means searches the IP database, reads out the descriptions of the output data structure definition portion of the first system level IP and the input data structure definition portion of the second system level IP, and generates the conversion circuit based on the read out descriptions.

4. The IP-based LSI design system according to claim 3,

wherein the IP database further comprises an IP for the communication channel; and

wherein, when the communication channel is provided between the first and the second system level IPs, the conversion circuit generating means searches the IP database and further reads out input/output data structure definitions of the IP for the communication channel.

5. The IP-based LSI design system according to claim 3,

wherein, when input/output data structures are different between the first and the second system level IPs, the conversion circuit generating means generates the conversion circuit in accordance with information representing a correspondence between the input/output data structures.

6. The IP-based LSI design system according to claim 2,

wherein the conversion circuit converts the amount of data per communication unit.

7. The IP-based LSI design system according to claim 2,

wherein the conversion circuit performs a conversion between address data indicating a data area and actual data corresponding to the address data.

8. An IP-based LSI design method, using an IP database having a system level IP used in system level design,

wherein, in the system level IP, each IP is described divided into:

a processing algorithm description portion describing a processing algorithm of the IP;
an input data structure definition portion representing a structure definition of input data serving as a processing unit; and
an output data structure definition portion representing a structure definition of output data serving as a processing unit.

9. The IP-based LSI design method according to claim 8,

comprising a step of generating a conversion circuit that converts data for communication between a communication channel and the system level IPs, when the communication channel is provided between the system level IPs performing data communication in architecture design or function design.

10. The IP-based LSI design method according to claim 9,

wherein, when the communication channel is provided between a first and a second system level IP communicating with each other, in the conversion circuit generating step, the IP database is searched, descriptions of the output data structure definition portion of the first system level IP and the input data structure definition portion of the second system level IP are read out, and the conversion circuit is generated based on the read out descriptions.

11. The IP-based LSI design method according to claim 10,

wherein the IP database further comprises an IP for the communication channel; and

wherein, when the communication channel is provided between the first and the second system level IPs, in the conversion circuit generating step, the IP database is searched and input/output data structure definitions of the IP for the communication channel are further read out.

12. The IP-based LSI design method according to claim 10,

wherein, when input/output data structures are different between the first and the second system level IPs, in the conversion circuit generating step, the conversion circuit is generated in accordance with information representing a correspondence between the input/output data structures.

13. The IP-based LSI design method according to claim 9,

wherein the conversion circuit converts the amount of data per communication unit.

14. The IP-based LSI design method according to claim 9,

wherein the conversion circuit performs a conversion between address data indicating a data area and actual data corresponding to the address data.

15. An IP-based LSI design system comprising:

a function classification database in which an equipment configuration is classified into respective elements with regard to function and arranged systematically,

wherein IP-based LSI design is carried out using the function classification database.

16. The IP-based LSI design system according to claim 15,

further comprising an existing design asset database in which IPs already generated are stored

in association with elements in the function classification database,

wherein an IP suitable for an LSI to be designed is selected from the IPs stored in the existing design asset database with reference to the function classification database.

17. The IP-based LSI design system according to claim 16,

further comprising a design assets compatibility evaluation rule database that stores information for defining mutual compatibility between the IPs stored in the existing design asset database,

wherein compatibility of the IP selected for the LSI to be designed is evaluated with reference to the design assets compatibility evaluation rule database.

18. The IP-based LSI design system according to claim 16,

wherein an IP having a similar function to that of an IP suitable for the LSI to be designed is selected from the IPs stored in the existing design asset database, and

wherein the function of the selected IP is revised so as to be suitable for the LSI to be designed.

19. The IP-based LSI design system according to claim 16,

wherein the existing design asset database comprises a means for managing history information, such as a progenitor IP and differences from the progenitor IP, for each of the IPs to be stored.

20. An IP-based LSI design method,

wherein IP-based LSI design is carried out using a function classification database in which an equipment configuration is classified into respective elements with regard to function and arranged systematically.

21. The IP-based LSI design method according to claim 20,

using an existing design asset database in which IPs already generated are stored in association with respective elements in the function classification database,

wherein an IP suitable for an LSI to be designed is selected from the IPs stored in the existing design asset database with reference to the function classification database.

22. The IP-based LSI design method according to claim 21,

using a design assets compatibility evaluation rule database that stores information for defining mutual compatibility between the IPs stored in the existing design asset database,

wherein compatibility of the IP selected for the LSI to be designed is evaluated with reference to the design assets compatibility evaluation rule database.

23. The IP-based LSI design method according to claim 21, wherein

an IP having a similar function to that of an IP suitable for the LSI to be designed is selected from the IPs stored in the existing design asset database, and

the function of the selected IP is revised so as to be suitable for the LSI to be designed.

24. An IP-based LSI design system comprising;

a means for generating architecture level design data from a system level function definition regarding an LSI to be designed;
a means for performing operation analysis of the LSI to be designed by using the generated architecture level design data and an operation pattern definition of the LSI to be designed; and
a means for generating a power control block in the architecture level design data based on operation analysis results.

25. An IP-based LSI design method comprising the steps of:

generating architecture level design data from a system level function definition;
performing an operation analysis of the LSI to be designed by using the generated architecture level design data and an operation pattern definition of the LSI to be designed; and
generating a power control block in the architecture level design data based on operation analysis results.

Fig. 1

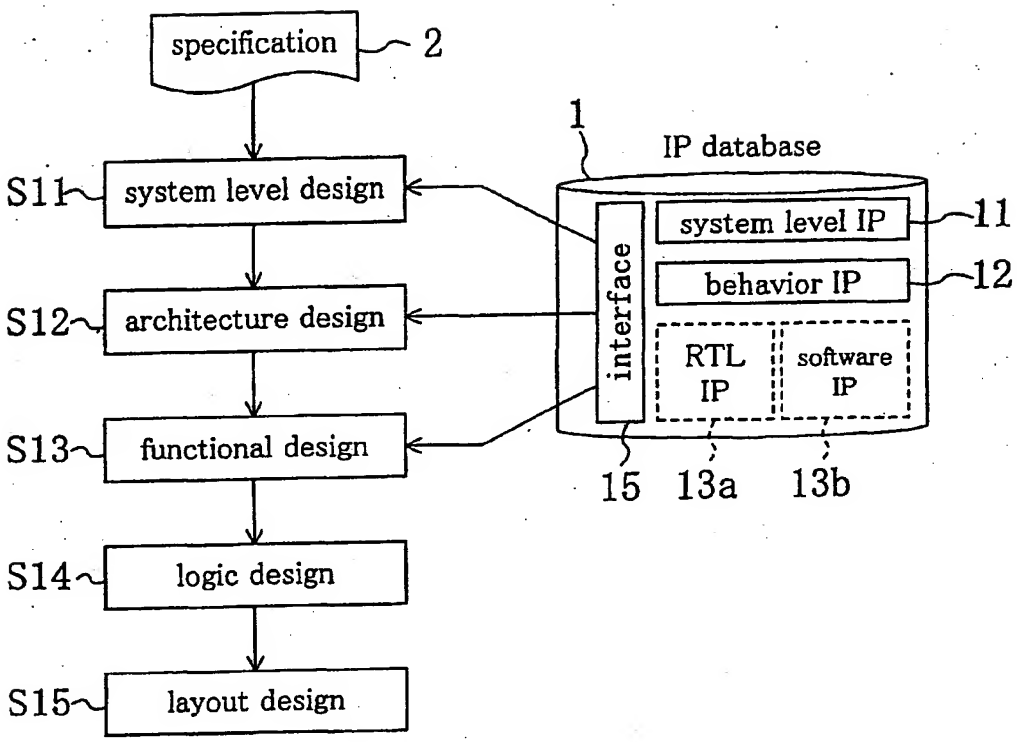

specification
2
1
IP database
S11
system level design
system level IP
11
S12
architecture design
behavior IP
12
interface
RTL IP
software IP
S13
functional design
15
13a
13b
S14
logic design
S15
layout design

Fig. 2(a)

system level

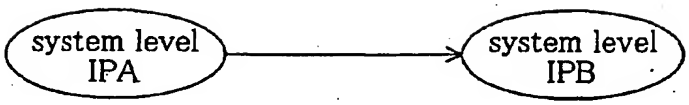


Fig. 2(b)

architecture level
functional level

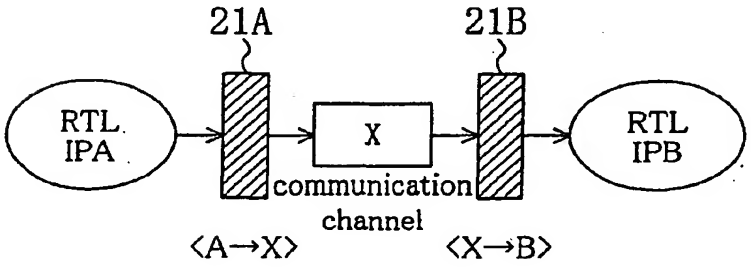


Fig. 3

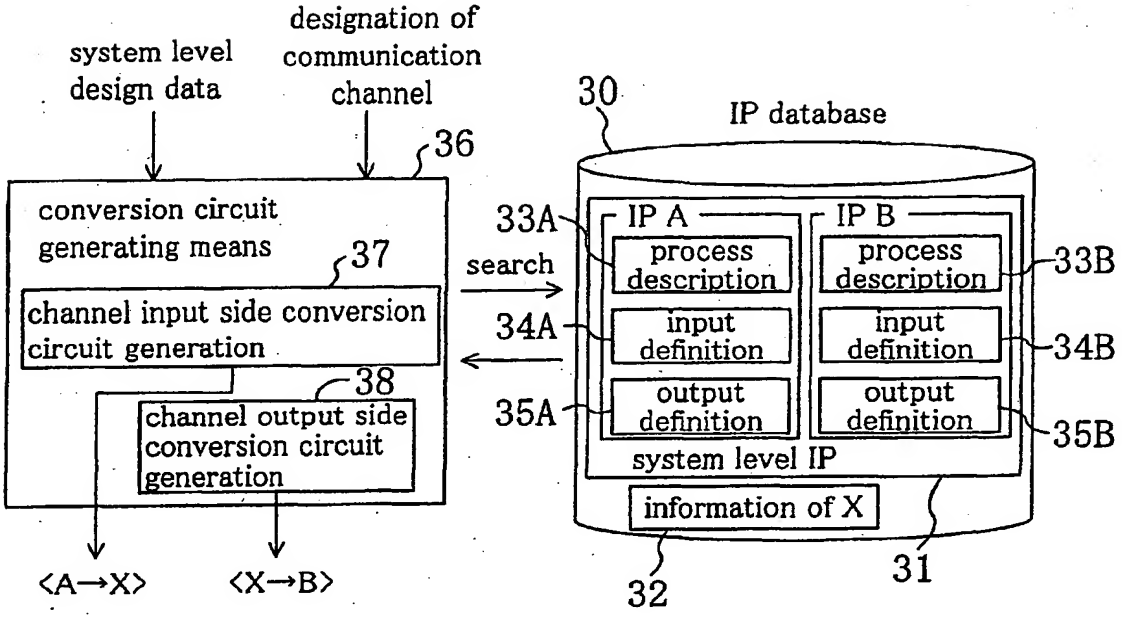


Fig. 4(a)

<A→X>

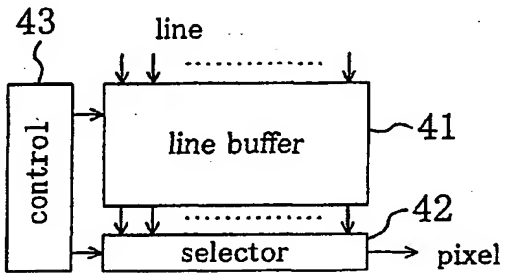


Fig. 4(b)

<X→B>

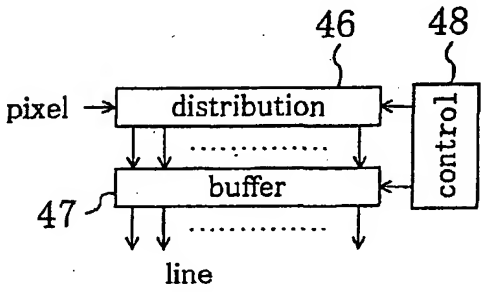


Fig. 5(a)

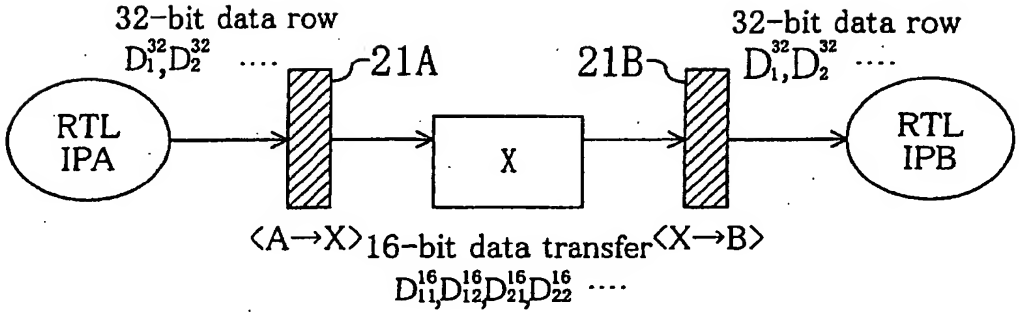


Fig. 5(b) <A→X>

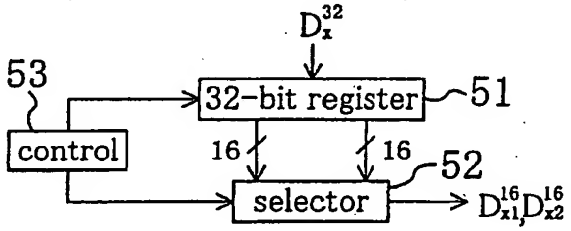


Fig. 5(c) <X→B>

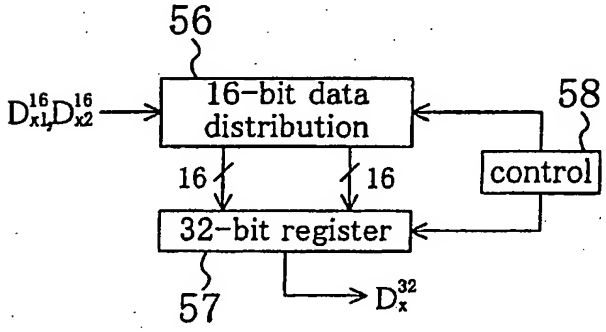


Fig. 6

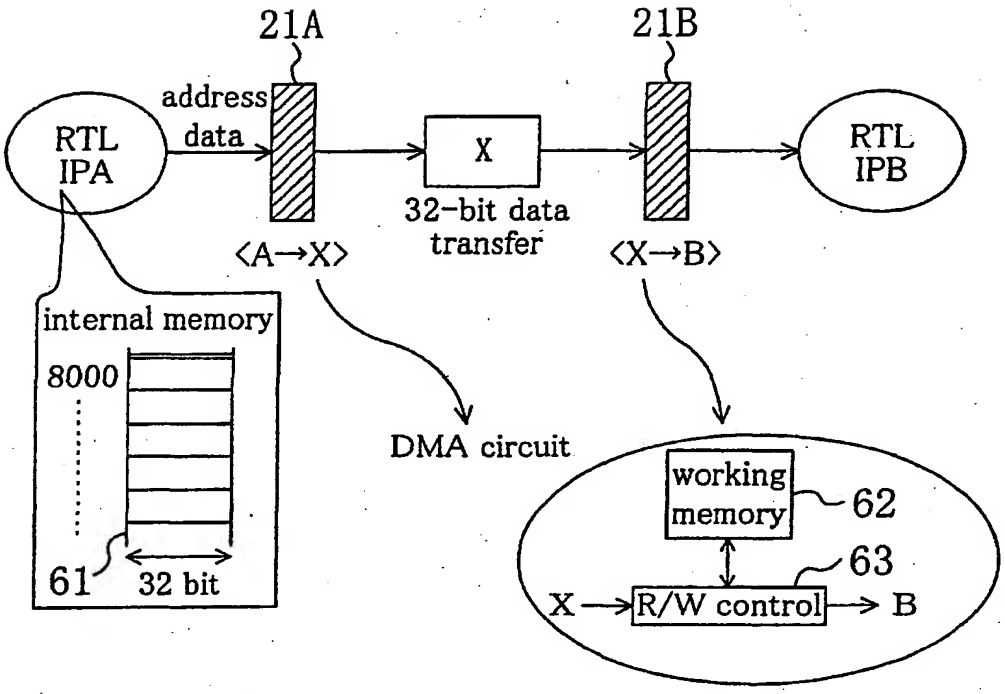
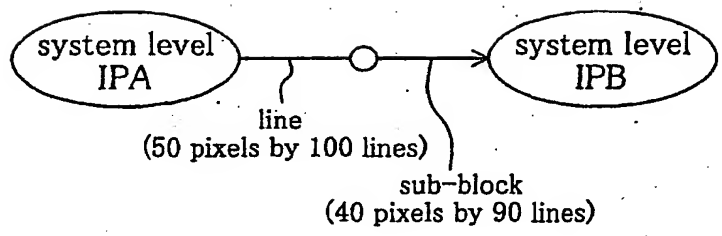
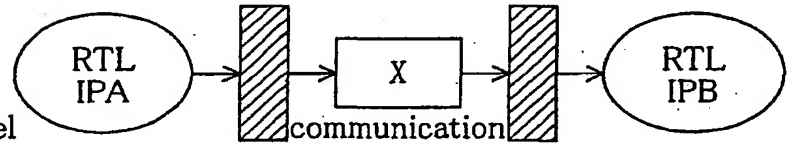

21A
21B
address
data
RTL
IPA
X
RTL
IPB
32-bit data
transfer
<A→X>
<X→B>
internal memory
8000
61
32 bit
DMA circuit
working
memory
62
63
X
R/W control
B

Fig. 7(a)



system level

Fig. 7(b)



architecture level
functional level

Fig. 8

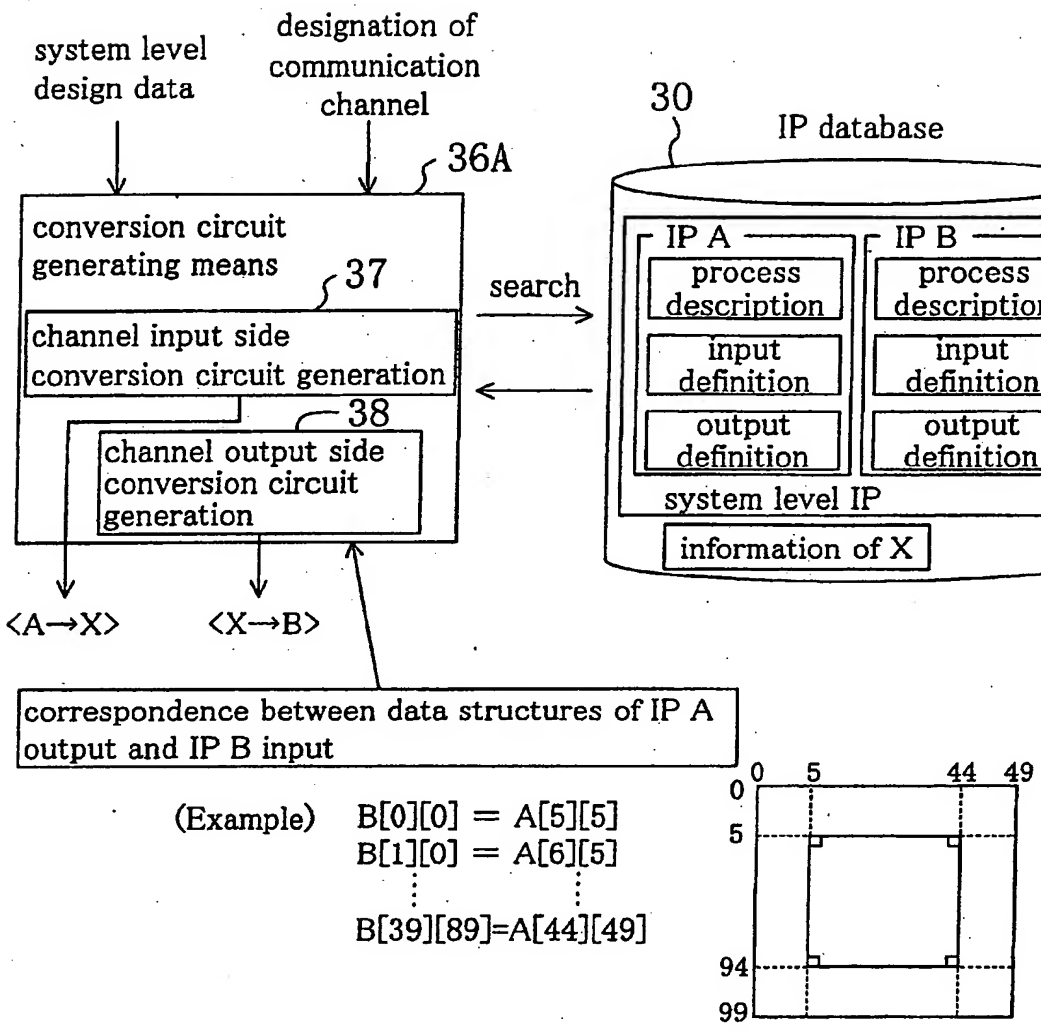

system level design data
designation of communication channel
36A
30
IP database
conversion circuit generating means
37
search
channel input side conversion circuit generation
38
channel output side conversion circuit generation
IP A
IP B
process description
input definition
output definition
process description
input definition
output definition
system level IP
information of X
<A→X>
<X→B>
correspondence between data structures of IP A output and IP B input
(Example) B[0][0] = A[5][5]
B[1][0] = A[6][5]
B[39][89]=A[44][49]
0
5
44
49
0
5
94
99

Fig. 9

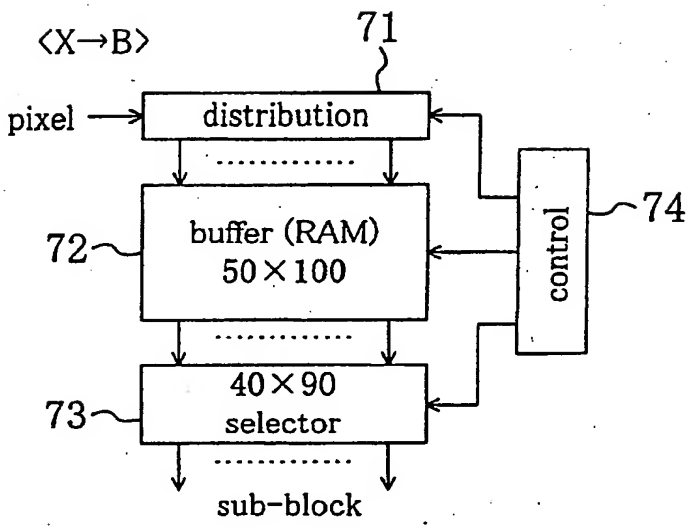

〈X→B〉
71
pixel
distribution
72
buffer (RAM)
50×100
74
control
73
40×90
selector
sub-block

Fig. 10

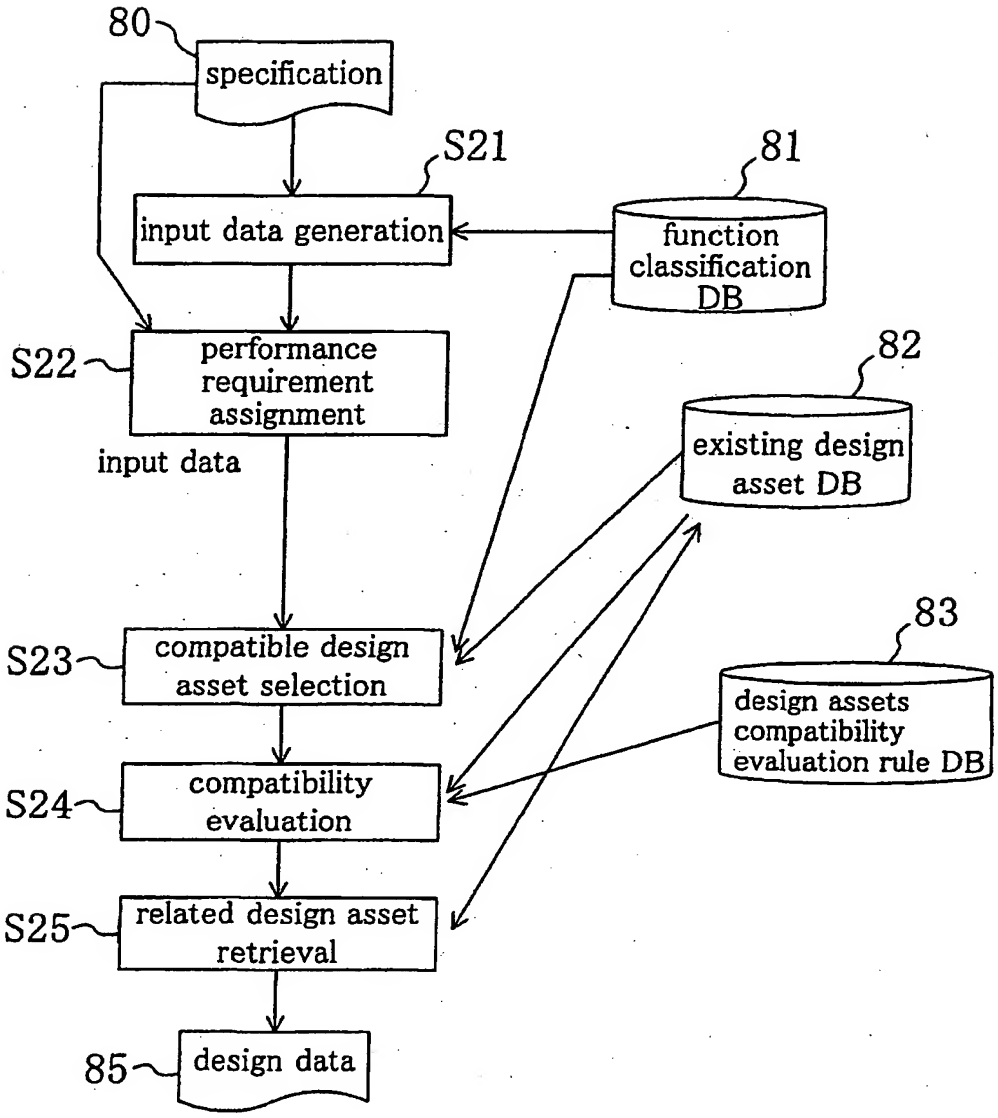

80
specification
S21
81
input data generation
function classification DB
S22
performance requirement assignment
82
existing design asset DB
input data
S23
compatible design asset selection
83
design assets compatibility evaluation rule DB
S24
compatibility evaluation
S25
related design asset retrieval
85
design data

Fig. 11

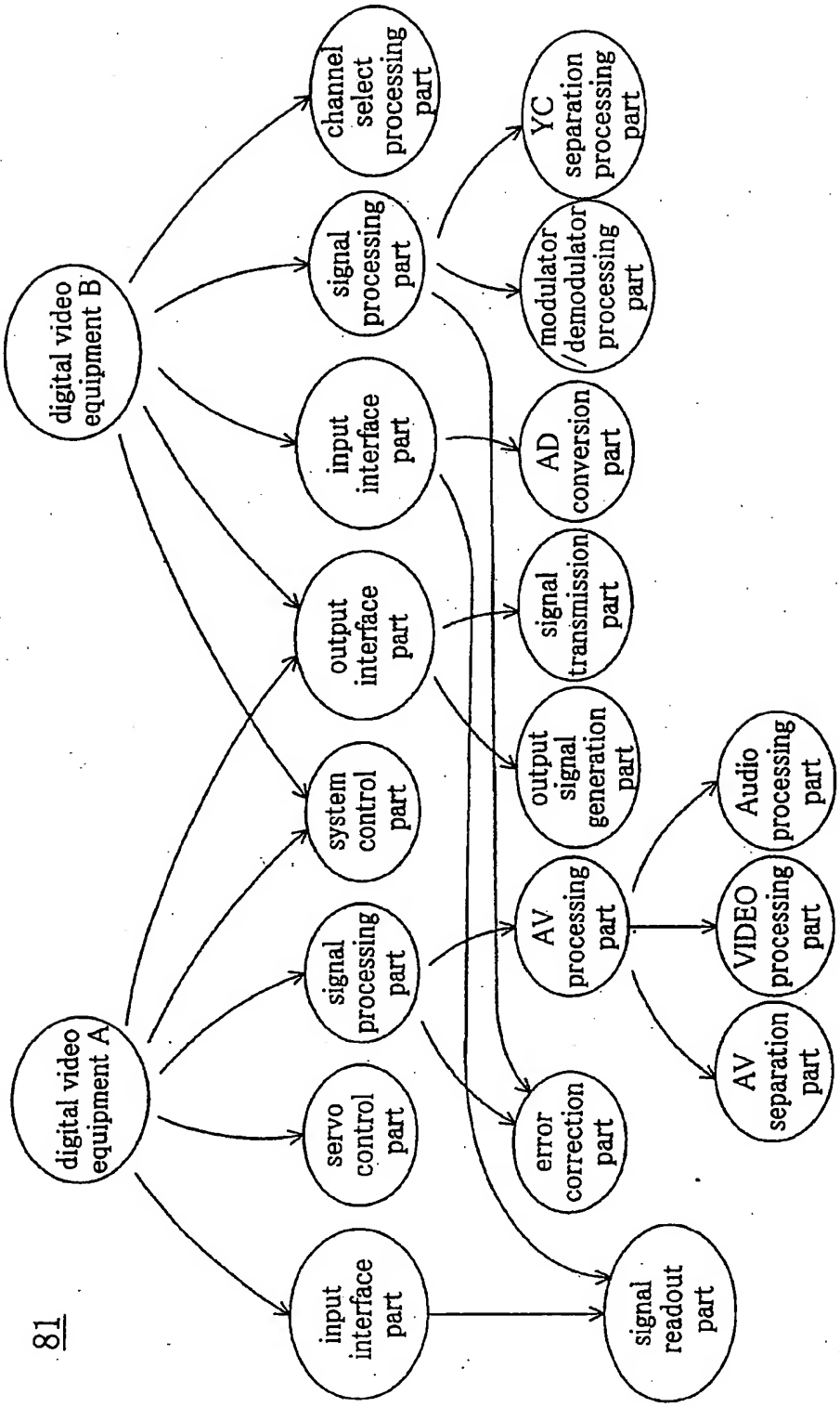

81
digital video equipment A
digital video equipment B
input interface part
servo control part
signal processing part
system control part
output interface part
input interface part
signal processing part
channel select processing part
error correction part
AV processing part
output signal generation part
signal transmission part
AD conversion part
modulator /demodulator processing part
YC separation processing part
signal readout part
AV separation part
VIDEO processing part
Audio processing part

Fig. 12

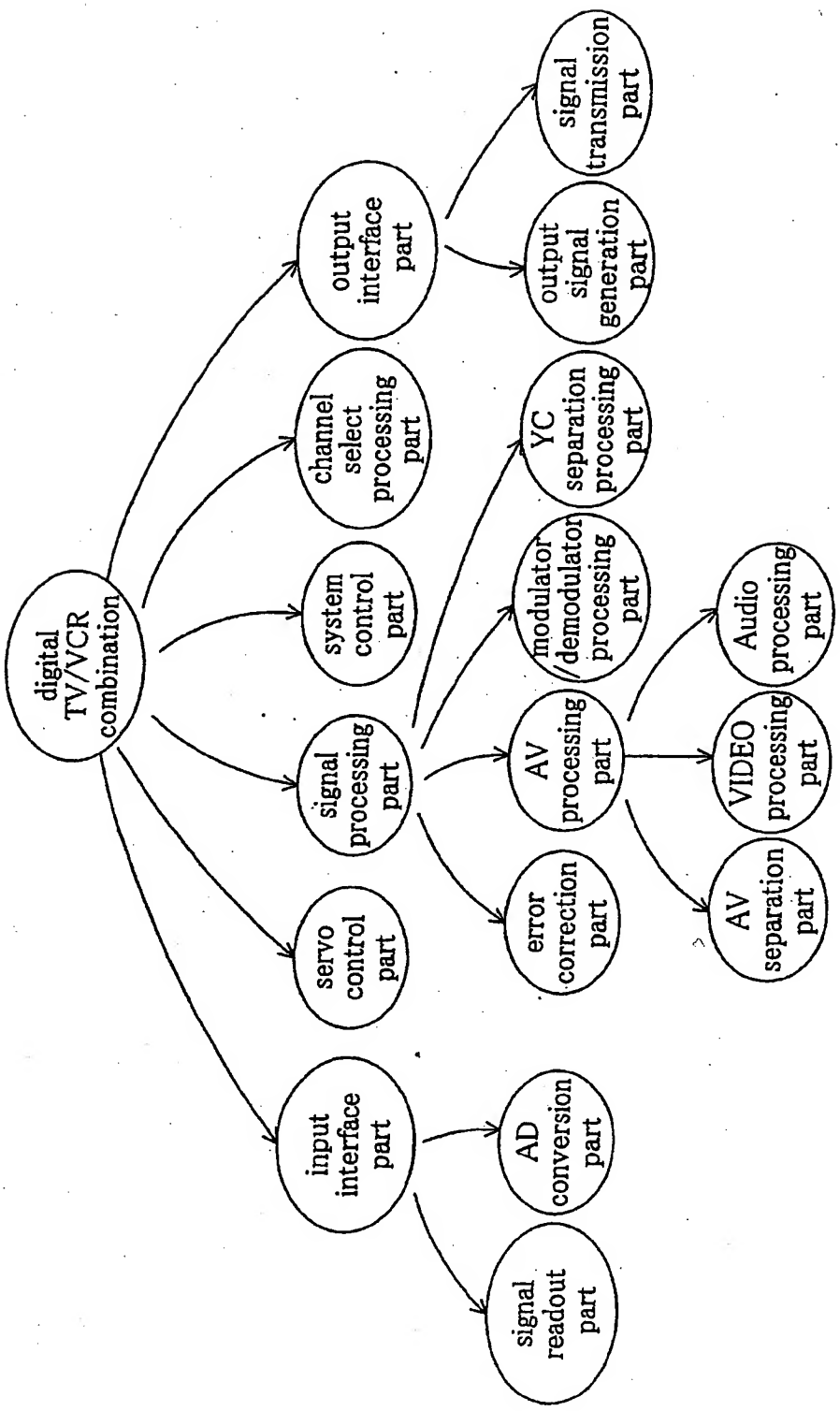

digital TV/VCR combination
input interface part
AD conversion part
signal readout part
servo control part
signal processing part
error correction part
AV processing part
modulator /demodulator processing part
YC separation processing part
AV separation part
VIDEO processing part
Audio processing part
system control part
channel select processing part
output interface part
output signal generation part
signal transmission part

Fig. 13

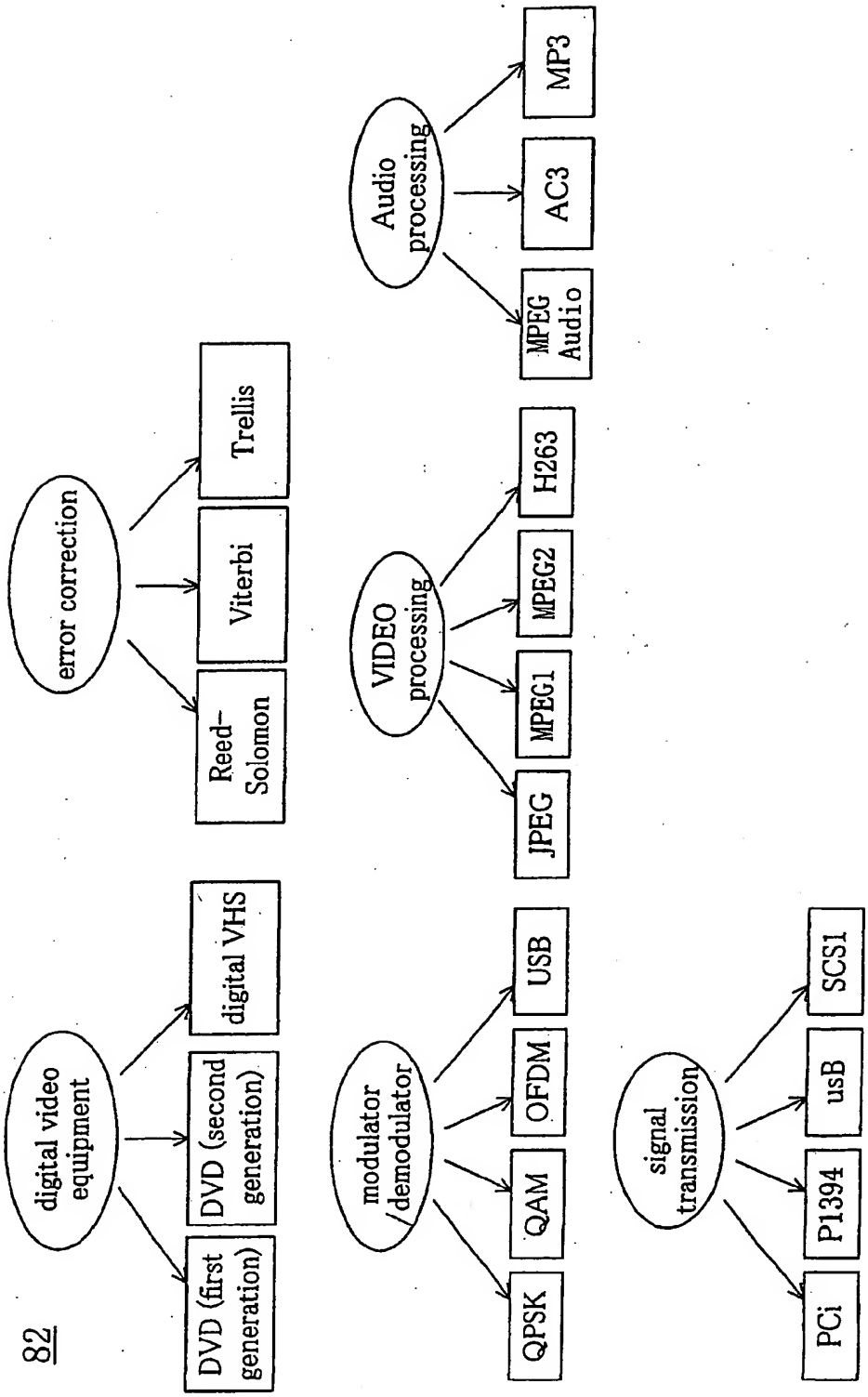
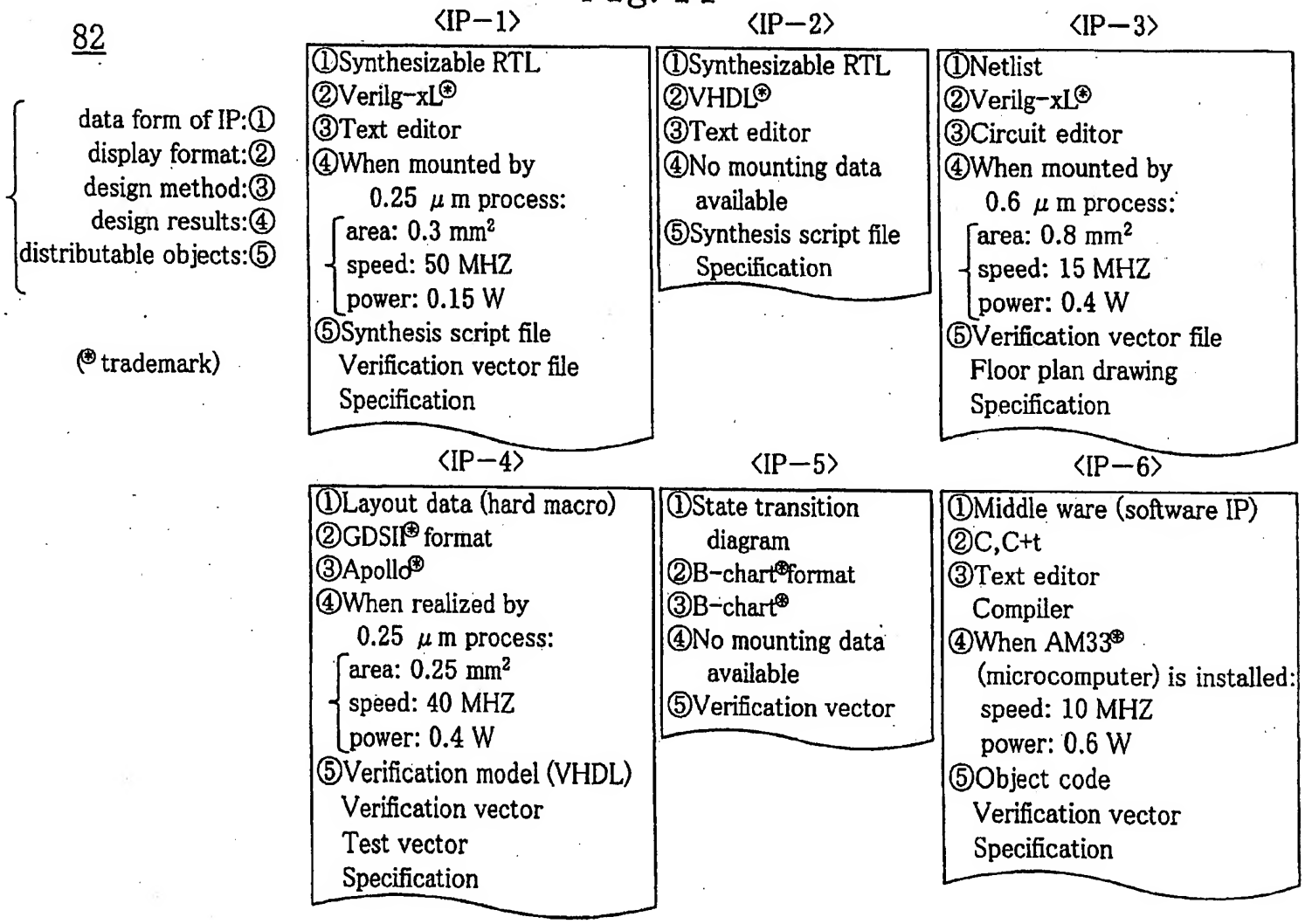

82
digital video equipment
DVD (first generation)
DVD (second generation)
digital VHS
error correction
Reed-Solomon
Viterbi
Trellis
modulator demodulator
QPSK
QAM
OFDM
USB
VIDEO processing
JPEG
MPEG1
MPEG2
H263
Audio processing
MPEG Audio
AC3
MP3
signal transmission
PCi
P1394
usB
SCS1

Fig. 14



EP 1 237 099 A1

83

Fig. 15

Combination of IPs	Compatibility
(IP-1) and (IP-2)	·An verification tool that can verify Verliog-xL and VHDL installed together is required. (theoretical)
(IP-1) and (IP-3)	·Verification time is increased. (theoretical) ·There are common blocks. ·When mounted by 0.18 μm: area: 0.2 mm^2, speed: 40 MHZ, power: 0.1 W. (empirical)
(IP-3) and (IP-4)	·An interface block between IPs is required. (empirical) ·When mounted by 0.25 μm: area: 0.5 mm^2, speed: 40 MHZ, power: 0.6 W. (empirical)
(IP-2) and (IP-3)	·Verification time is increased. (theoretical)
(IP-4) and (IP-6)	·IP-6 can be installed in IP-4. (empirical) ·Performance when installed: speed: 10 MHZ, power: 0.6 W. (empirical)
(IP-1) and (IP-5)	·Same functionality. (theoretical)
(IP-2) and (IP-4) and (IP-5)	·When mounted by 0.18 μm: area: 0.3 mm^2, speed: 20 MHZ, power: 0.5 W. (empirical)
⋮	

Fig. 16

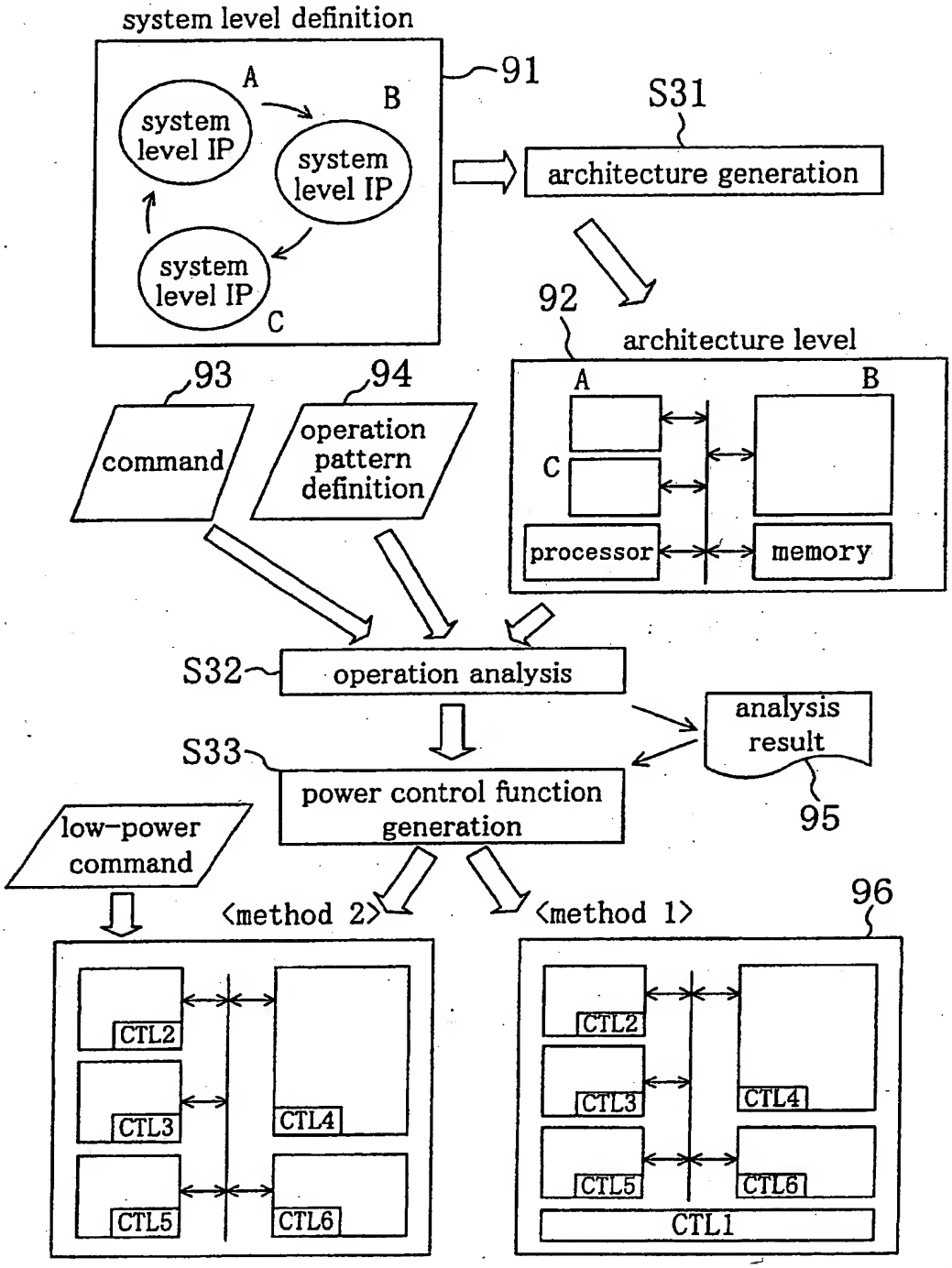
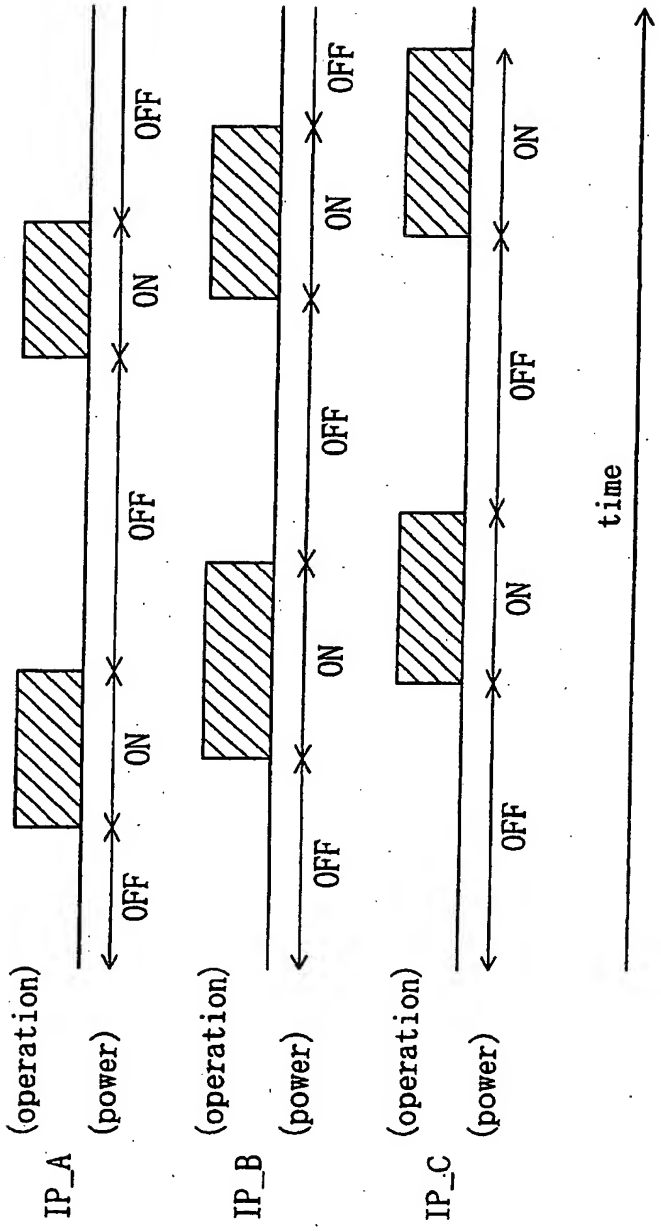

system level definition
A
B
C
system level IP
system level IP
system level IP
91
S31
architecture generation
92
architecture level
A
B
C
processor
memory
93
command
94
operation pattern definition
S32
operation analysis
analysis result
95
S33
power control function generation
low-power command
<method 2>
<method 1>
96
CTL2
CTL3
CTL4
CTL5
CTL6
CTL1

Fig. 17


IP_A
(operation)
(power)
OFF
ON
OFF
IP_B
(operation)
(power)
OFF
ON
OFF
IP_C
(operation)
(power)
OFF
ON
OFF
time

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/07869

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] G06F17/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] G06F17/50, H01L21/82

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-2000
Kokai Jitsuyo Shinan Koho 1971-2000 Jitsuyo Shinan Toroku Koho 1996-2000

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	EP, 674285, A2 (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.), 27 September, 1995 (27.09.95),	
X	Column 6, lines 47 to 58; Fig. 2	1,8
A	Column 6, lines 47 to 58; Fig. 2	2-7,9-14
Y	Column 11, line 15 to Column 16, line 55; Figs. 9-14 & JP, 7-311797, A	16-18,21-23
	EP, 584828, A2 (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.), 02 March, 1994 (02.03.94),	
X	Column 18, line 54 to Column 28, line 23; Figs. 15 to 24	15,20
Y	Column 18, line 54 to Column 28, line 23; Figs. 15 to 24	16-18,21-23
A	Column 18, line 54 to Column 28, line 23; Figs. 15 to 24 & JP, 6-332965, A	19
X	NEC Gihou, Vol. 50, No.3, March 1997 (Japan), Katsuya FURUKI et al., "System LSI Sekkei System Open CAD (V5)", pp.98-102 , especially, p.101, right column, line 25-40	24,25

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 December, 2000 (20.12.00)	16 January, 2001 (16.01.01)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/07869

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 7-129657, A (NEC Corporation), 19 May, 1995 (19.05.95), Full text; all drawings (Family: none)	15-23

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/07869

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

The inventions of claims 1-14 relate to an idea of designing a system performing data communication, the inventions of claims 15-23 relate to an idea of designing using a function classification database, and the inventions of claims 24, 25 relate to an idea of creating a power control block.

These three groups of inventions are not for achieving the same unsolved object and have no common essential technical matters. Therefore these groups of inventions are not so linked as to form a single general inventive concept.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest
☐ The additional search fees were accompanied by the applicant's protest.
☒ No protest accompanied the payment of additional search fees.

Form PCT/ISA/210 (continuation of first sheet (1)) (July 1992)